Tutorial 7
Some Combinational Circuits

Exercise 1

Full Adder

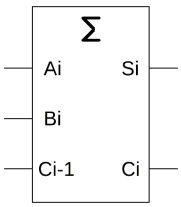


Figure 1

4-bit Adder

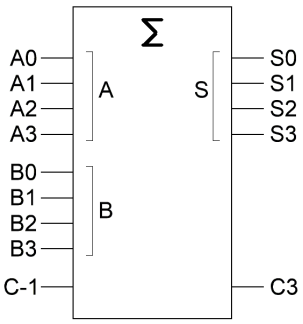


Figure 2

Adder-Subtractor

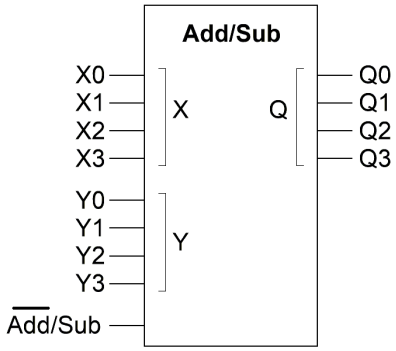


Figure 3

First, we want to create a full adder (see figure 1) that adds two bits (Ai and Bi) and a possible carry input (Ci-1). This circuit generates a sum (Si) and a possible carry output (Ci).

1. Give the truth table of this circuit.
2. Give the expression of Si and simplify it using the algebraic method.
3. Give the simplest expression of Ci using a Karnaugh map.
4. Draw the circuit diagram of the full adder.

Next, we want to create a 4-bit adder (see Figure 2) that adds two 4-bit words (A and B) and a possible carry input (C-1). This circuit generates a 4-bit sum (S) and a possible carry output (C3).

5. Draw the circuit diagram of the 4-bit adder using four full adders.

Finally, we want to design a 4-bit adder-subtractor (see Figure 3) that adds or subtracts two 4-bit words (X and Y). If the $\overline{\text{Add}}$/Sub input is 0, the Q output contains the sum. If the $\overline{\text{Add}}$/Sub input is 1, the Q output contains the difference (X – Y). For simplicity, this circuit will not include the carries.

6. Let us consider a circuit with two inputs (N and D) and one G output. If the N input is 0, then the G output is equal to D. If the N input is 1, then the G output is equal to $\overline{\text{D}}$. Find the logic gate that corresponds to this circuit.

7. Let us consider a circuit with a D input that is made up of four bits (D0, D1, D2, and D3), one inversion input (I), and a G output, that is made up of four bits (G0, G1, G2, and G3). If the I input is 0, then the G output is equal to D (G0 = D0, G1 = D1, G2 = D2, G3 = D3). If the I input is 1, then the G output is equal to the one's complement of D (G0 = $\overline{D0}$, G1 = $\overline{D1}$, G2 = $\overline{D2}$, G3 = $\overline{D3}$). Implement this circuit using the gate determined in the previous question.
8. Given that A – B can be replaced by A + C2(B), and that C2(B) = C1(B) + 1, draw the circuit diagram of the adder-subtractor using a 4-bit adder and the circuit from the previous question. Note: C2 = Two's complement; C1 = One's complement.

Exercise 2

1-bit Comparator

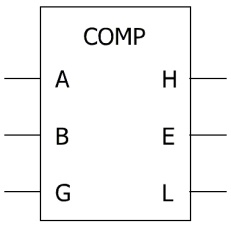


Figure 1

4-bit Comparator

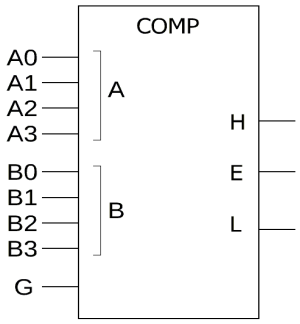


Figure 2

7-Segment Decoder

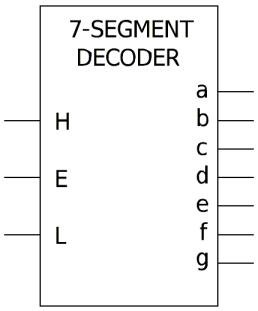


Figure 3

First, we want to design a 1-bit comparator (see figure 1) with the following inputs and outputs:

- Inputs: a strobe override (*G*), two bits to compare (*A* and *B*).
- Outputs: higher (*H*), equal (*E*), lower (*L*).

If $G = 0$: $H = E = L = 0$ (*A* and *B* are ignored)
If $G = 1$: $A > B \rightarrow H = 1, E = 0, L = 0$
$A = B \rightarrow H = 0, E = 1, L = 0$
$A < B \rightarrow H = 0, E = 0, L = 1$

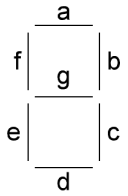
1. Give the truth table of this circuit.
2. Write down the most simplified expressions of *H*, *E* and *L*.
3. Draw the circuit diagram of the 1-bit comparator.

Now, we want to design a 4-bit comparator (see figure 2) that compares two unsigned numbers. Its behavior should be similar to the 1-bit comparator apart from the 4-bit inputs: *A* (*A3*, *A2*, *A1*, *A0*) and *B* (*B3*, *B2*, *B1*, *B0*).

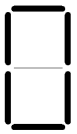
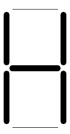
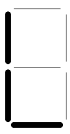
4. Using four 1-bit comparators and some logic gates, draw the circuit diagram of the 4-bit comparator.

Finally, we want to display the outputs of the 4-bit comparator using a 7-segment display. To do so, we need to design a 7-segment decoder (see figure 3).

7-segment display



If the value of a segment is 1, the associated LED is on; otherwise, it is off.

Display for the 4-bit comparator			
			
$G = 0$	$A > B$	$A = B$	$A < B$

5. Draw the truth tables of the seven segments (a, b, c, d, e, f, g) in terms of H, E and L.
6. Write down the most simplified expressions of the seven segments.
7. Draw the circuit diagram of the 7-segment decoder.